

Appl. No. 09/405,210
Amdt. dated May 16, 2003
Reply to Office Action of [date]

PATENT

REMARKS/ARGUMENTS

The present response is submitted in accordance with the Revised Amendment Format as set forth in the Notice provided on the USPTO web site for the Office of Patent Legal Administration; Pre-OG Notices; signed 1/31/03.

Upon entry of this Response, claims 1-3, 6-8, 12-15, and 18-21 remain pending. Claims 1-3, 6-8, 12-15, 19, and 21 were rejected under 35 U.S.C. §102(e) as being anticipated by Witek, U.S. Patent No. 6,037,202. Claims 18 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Witek in view of Murakami, U.S. Patent No. 5,177,572.

Reconsideration in view of the following remarks is respectfully requested.

It should be noted that the present amendment does not modify the claims. The replacement listing above incorporates changes made in previous amendments and is provided for the Examiner's convenience.

Rejection of Claims 1-3, 6-8, 12-15, 19, and 21 under 35 U.S.C. §102(e)

Claims 1-3, 6-8, 12-15, 19, and 21 were rejected under 35 U.S.C. §102(e) as being anticipated by Witek, U.S. Patent No. 6,037,202. Applicants respectfully traverse.

Independent claim 1 is directed to a method of manufacturing a trench field effect transistor on a substrate. A first trench is formed and filled with conductive material to form a gate electrode. A body region and a source region are formed in the substrate. A second trench is formed adjacent to the source region, terminating in contact with the body region. The second trench is filled with high conductivity material making contact to the body region. As described in this specification, the second trench acts as a heavy body to improve transistor ruggedness and performance.

In contrast, Witek discloses a method for forming a trench transistor structure in which two serially connected transistors with a common current electrode (12) are formed on either sides of the same trench (see Witek, Abstract, and col. 5, lines 12-28). Use of this method to form a six-transistor static random access memory (SRAM) cell is described in connection with Figs. 23-34, on which the rejection relies, and a circuit schematic of the resulting RAM cell

is shown in Fig. 35. Applicants note that no disclosure related to "a body region" (e.g., region 108 in Figs. 2A and 2B of the present application) or "a second trench" (e.g., region 200 in Figs. 2A and 2B of the present application) could be found in Witek. Nor could there be found any disclosure of "forming a source region ... inside the body region" anywhere in Witek, or of forming the second trench "adjacent to said source region" where the source region is of opposite conductivity as compared to the "body region."

As explained in Witek (col. 11, lines 15-35), the structure shown in Fig. 32 provides three transistors of the six-transistor SRAM cell of Fig. 35. Transistor 500 is an N-channel transistor having current electrodes 126 and 101 and gate electrode 114; its body region is the portion of the substrate that lies between layers 126 and 101. Transistor 502 is a P-channel transistor having current electrodes 103 and 124 and gate electrode 114; its body region is layer 104 (col. 11, lines 23-28). Transistor 504 is an N-channel transistor having current electrodes 128 and 101 and gate electrode 116; its body region is the portion of the substrate that lies between layers 128 and 101 (col. 11, lines 28-34).

The center trench shown in Fig. 32 filled with conductive layer 140 is used to perform the cross-coupling between the three-transistor structures. [Witek, col. 13, lines 42-56]. This trench does not act as a heavy body as set forth in claim 1. Fig. 35 shows that transistors 500, 502, 504 are coupled at a common terminal to a signal path 148. In Fig. 32, buried layer 101 provides the common terminal for these three transistors (cf. Fig. 9; col. 5, lines 13-17). To provide an electrical contact for buried layer 101 at the surface of the device, a third trench is formed and partially filled with conductive material 140. As shown in Fig. 34, the top surface of conductive layer 140 is used as a connection point for a metal interconnect 148 (col. 11, lines 61-63). Thus, the third trench (referred to herein as an electrode trench) is not a heavy body at all.

Because the entire structure and in particular the cross-coupling electrode trench in the Witek device is fundamentally different from that trench transistor and in particular the "second trench" recited in claim 1, the method disclosed in Witek differs from the method recited in claim 1 of the present application in several significant respects.

First, claim 1 recites a step of "substantially filling the first trench with conductive material to form a gate electrode of the field effect transistor." Witek does not teach or suggest

that either gate trench is substantially filled with a conductive material. Instead, as shown in Fig. 26, the gate trenches are lined with annular spacers 114, 116 of conductive material (col. 9, lines 33-36). The gate trenches are then filled with dielectric 118, 120 (col. 10, lines 1-3). Thus, the gate trenches in Witek are not substantially filled with conductive material as recited in claim 1; instead, they are lined with conductive material and then filled with dielectric material.

Second, claim 1 recites "forming a body region having a second conductivity type in the substrate." It is not clear from the rejection what area of the Witek structure the rejection finds to correspond to the claimed "body region." The rejection states on page 3 that Witek discloses "etching a second trench through the source region and into the body region 101" while identifying the source regions as 126/128 in the line above. Claim 1, however, clearly recites that the "source region" is formed "inside the body region." As shown in Fig. 32 of Witek, source regions 126/128 are clearly not formed "inside" buried layer 101. This inconsistency is due to the fact that the Witek device has not region that would functionally correspond to the claimed "body region."

Third, claim 1 recites a step of "forming a second trench adjacent to said source region, the second trench defined by sidewalls extending into the body region and a bottom, which terminates below the source region and in contact with the body region." None of the trenches in Witek including the electrode trench (i.e., the trench filled with dielectric 138 and conductive material 140) has the features as set forth in claim 1. For instance, the electrode trench terminates in contact with layer 101, which is a current electrode of the transistors (as explained above), not a body region of any transistor. In addition, the electrode trench is clearly not adjacent to the source regions 126, 128 of the N-channel transistors, and it is isolated from source region 124 of the P-channel transistor by dielectric layer 138. Furthermore, source region 124 is of the same conductivity type (P type) as the substrate whereas the claimed source region has a "second conductivity type." Thus, the electrode trench is not "adjacent to said source region" and does not "terminate[] ... in contact with the body region" as recited in claim 1.

Fourth, claim 1 recites a step of "filling the second trench with high conductivity material for making contact to the body region." Witek also does not disclose or suggest this step. The electrode trench is first lined with a dielectric spacer 138 to isolate regions 124, 104,

and 103 (col. 11, lines 3-5). Then a conductive layer 140 is deposited (col. 11, lines 9-11). To the extent that region 104 can be characterized as a body region for P-channel transistor that is formed by regions 124/104/103, dielectric spacer 138 prevents conductive layer 140 from making contact with the body region 104 of the P-channel transistor or any other body region. Thus, Witek also fails to teach or suggest that the high conductivity material "mak[es] contact to the body region" as recited in claim 1.

For at least these reasons, claim 1 is patentable over Witek, and claims 2, 3, 6-8, 12, and 19, which depend from claim 1, are also patentable over Witek. These claims also recite additional optional features of the invention that further distinguish over Witek.

For instance, claim 2 recites that the high conductivity material "also makes contact to the source region." In Witek, conductive layer 140 is insulated by dielectric 138 and does not make contact to source region 124 of the P-channel transistor or any other source region. Claim 2 is patentable over Witek for this reason also.

Claim 6 recites an additional step of "forming a thin layer of barrier metal between the high conductivity material and the body region." Claim 7 recites specific choices for the high conductivity material (aluminum) and barrier metal (titanium). Witek shows only dielectric 138 (which is not metal) between conductive material 140 and body region 104. Witek does not disclose or suggest providing a layer of barrier metal as recited in claim 6, let alone the specific choice of titanium recited in claim 7. Claims 6 and 7 are patentable for at least these reasons also.

Independent claim 13 recites elements similar to the elements of claim 1 discussed above, including steps of "substantially filling the first trench with polysilicon" (a conductive material); "etching a second trench through the source region and into the body region, the second trench defined by sidewalls and a bottom, which terminates in contact with the body region"; and "filling the second trench with metal making contact with both the source region and the body region." Therefore, the foregoing arguments with regard to claim 1 apply with equal force to claim 13. In addition, it is noted that Witek does not teach or suggest that the conductive material 140 makes contact with the source region of any transistor; dielectric layer 138 prevents any such contact.

For at least these reasons, claim 13 is patentable over Witek, and claims 14, 15, and 21, which depend from claim 13, are also patentable over Witek.

Claim 14 also recites "implanting impurities of the second conductivity type into the body region under the second trench before the step of filling the second trench with metal." Witek discloses that impurities can be implanted into an optional N region 136 (shown in Fig. 32) under the electrode trench, but N region 136 is not in the body region of any transistor. Instead, it is provided "to ensure that electrical contact is made to buried layer 101" (col. 11, lines 7-11), which corresponds to a current electrode, not a body region. Claim 14 is patentable over Witek for at least this reason also.

Claim 15 recites that "the step of etching the second trench etches the second trench to a shallower depth than the first trench." This feature is also not taught or suggested by Witek. The electrode trench terminates in contact with buried layer 101 so that signals from that node can be propagated on line 148 as shown in Figs. 34 and 35. This suggests that the second trench should be deeper than the first trench, not shallower as recited in claim 15. Claim 15 is patentable over Witek for this reason also.

In view of the foregoing, withdrawal of the rejection of claims 1-3, 6-8, 12-15, 19, and 21 is respectfully requested.

Rejection of Claims 18 and 20 under 35 U.S.C. §103(a)

Claims 18 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Witek in view of Murakami, U.S. Patent No. 5,177,572. Applicants respectfully traverse.

First, the rejection of claims 18 and 20 relies on the assertion that Witek discloses all features of their parent claims (claims 1 and 13, respectively). As discussed above, this assertion is inaccurate in numerous significant respects.

Moreover, motivation to combine Murakami with Witek is lacking. Murakami is directed to Schottky junction devices, which are very different in structure and operational characteristics from ohmic devices such as those described in Witek that are designed for use in an SRAM cell. As just one example, note that the transistors described in Witek (as well as in

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the present application) include a body region having a second conductivity type, while the devices of Murakami lack such a region (see, e.g., Fig. 3; col. 6, lines 18-25). Given the significant differences between Schottky and transistors for use in an SRAM cell, persons of ordinary skill in the art would not have been motivated to combine Murakami with Witek.

For at least these reasons, claims 18 and 20 are patentable over Witek and Murakami. Withdrawal of the rejection of claims 18 and 20 is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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